CLAIM SUMMARY

1. (Presently amended) A method of forming a capacitor in an integrated circuit, the method comprising:

forming a first non-single-crystalline layer on a gate dielectric layer on a surface of a substrate of an integrated circuit;

forming a capacitor dielectric layer on the first non-single-crystalline layer;

forming a second non-single-crystalline layer on the capacitor dielectric layer;

removing portions of the second non-single-crystalline layer to define a top plate of the capacitor;

forming a mask over the top plate and exposed portions of the capacitor dielectric layer with an opening;

etching using the mask to simultaneously ~~removing~~ remove portions of the capacitor dielectric layer ~~to define a dielectric of the capacitor;~~ and

~~removing~~ portions of the first non-single-crystalline layer to define a bottom plate of the capacitor after a top plate is defined on the gate dielectric layer.

2. (Original) The method according to claim 1, wherein portions of the first non-single-crystalline layer are removed to simultaneously define a gate of a transistor of the integrated circuit.

3. (Original) The method according to claim 1, including forming a mask over the second non-single-crystalline layer with an opening and etching to remove the portions of the second non-single-crystalline layer.

4.-8 (Cancelled)

9. (Currently Amended) The method according to claim 1~~8~~, subsequent to the masking and etching, using the top plate as a mask and etching to remove additional portions of the capacitor dielectric layer to define the dielectric of the capacitor.

10. (Cancelled)

11. (Cancelled)

12. (Currently Amended) The method according to claim ~~11~~ 1, including forming a top dielectric layer over the defined first and second plates and the capacitor dielectric and forming contact vias to the first plate through the top dielectric and the capacitor dielectric and to the second plate through the top dielectric.